GP 1765
#3
Bell
9.1.00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kazuhiko TAKADA

Serial No.: 09/528,296

Filed: March 17, 2000 Examiner: Not yet assigned

For: SEMICONDUCTOR DEVICE HAVING A GUARD RING

INFORMATION DISCLOSURE STATEMENT PURSUANT TO 37 CFR 1.97(b)

Director of Patents and Trademarks
Washington, D.C. 20231

May 25, 2000

Sir:

The attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached Form PTO-1449. One copy of each of these documents is attached.

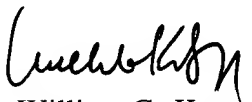
No fee or certification is required in connection with this Information Disclosure Statement, since it is being submitted prior to the issuance of a first official action on the merits or expiration of the three month period following filing of the above-captioned application.

The above information is presented so that the Patent and Trademark Office can, in the first instance, determine any materiality thereof to the claimed invention. See 37 CFR 1.104(a) concerning the PTO duty to consider and use any such information. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the documents cited in the attached Form PTO-1449 be made of record therein and appear on the first page of any patent to issue therefrom.

The Commissioner is authorized to charge our Deposit Account No. 01-2340 for any fee which is deemed by the Patent and Trademark Office to be required to effect consideration of this statement.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON



William G. Kratz, Jr.
Attorney for Applicant
Reg. No. 22,631

Atty. Docket No. 000294
1725 K Street, N.W., Suite 1000
Washington, DC 20006
Tel: (202) 659-2930
Fax: (202) 887-0357
WGK/nrp

Enclosures: PTO-1449 and 1 reference

INFORMATION DISCLOSURE STATEMENT

Japanese Laid-Open Patent Publication 7-201855, a full translation thereof being attached herewith, describes a guard ring pertinent to the present invention.

LAID-OPEN PATENT PUBLICATION (A)

LAID-OPEN NUMBER	7-201855
LAID-OPEN DATE	August 4, 1995
APPLICATION NUMBER	5-336434
FILING DATE	December 28, 1993
APPLICANT	Fujitsu, Co. Ltd. Fujitsu VLSI, Ltd.
INVENTOR	Ahikiro IWASE Eisaku ITOH Shinji NAGAI
ATTORNEY	Sadakazu IGETA

[TITLE OF THE INVENTION] SEMICONDUCTOR DEVICE

[ABSTRACT]

[PURPOSE] This invention is related to a semiconductor device having an elongate conductor film for improving moisture resistance such as a guard ring in a region between a rim of a semiconductor chip and a wiring pad. The purpose of the invention is to improve moisture resistance by improving the performance degradation caused by cracking, by reducing the external stress applied to the guard ring during the molding process of the semiconductor chip and causing a crack in the guard ring.

[CONSTRUCTION] A guard ring 4 of a conductor film 3 provided in a region between a rim of a semiconductor chip 1 and a wiring pad 2 is formed of a zigzag or curved pattern.

[CLAIMS]

[CLAIM 1] A semiconductor device in which a gurad ring (4) provided in a region between a rim of a semiconductor chip (1) and a wiring pad (2) has a zigzag or curved pattern.

[CLAIM 2] The semiconductor device of claim 1 wherein the guard ring (4) is formed of plural layers of conductor films (3), and wherein the conductor films (3) are interconnected with each other via a through-hole in an interlayer insulation film (7).

[CLAIM 3] The semiconductor device of claim 1 or 2, wherein the plural layers of conductor films (3) are stacked such that at least an upper conductor film (3) covers a lower conductor film (3b).

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[INDUSTRIAL FIELD OF THE INVENTION] The present invention relates to a semiconductor device having an elongate conductor film around a rim of a semiconductor substrate, such as the technology of forming a guard ring used for improving moisture resistance.

[0002]

[PRIOR ART] FIG.3 shows a conventional art. In the drawing, 1 is a semiconductor chip, 2 is a wiring pad, 3 is a conductor film, 4 is a gurad ring, 9 represent four corners

and 10 is a slit.

[0003] Conventionally, it is known that there occurs a cracking in the passivation film not illustrated formed so as to cover the conductor film 3 covering the guard ring 4 provided along a rim of the semiconductor chip 1 and the neighbourhood of the guard ring 4, due to the strong stress caused by the mold resin which tends to concentrate at the four corners of the semiconductor chip 1, provided that the guard ring 4 is formed of a straight conductor pattern 3 located in the region between the rim of the semiconductor chip 1 and the wiring pad 2 as represented in FIG.3(a).

[0004] Thus, the Japanese Laid-Open Patent Publication 2-77132 teaches an improvement of the foregoing drawback by providing a slit 10 in the guard ring 4 so as to extend parallel to the direction of the guard ring 4.

[0005]

[MEANS OF SOLUTION OF THE PROBLEM] On the other hand, the width of the guard ring has become very small due to the miniaturization of the semiconductor device. Due to the excessively small wiring width caused by the formation of the slit, the guard ring is tend to be disconnected due to the cracking of the passivation film, which is contrary to the purpose of the invention.

[0006] The present invention is made in view of the

problems noted above and has an object to provide a semiconductor device in which the problem of performance degradation or moisture resistance caused by the cracking of the passivation film on the guard ring due to the external stress, is improved.

[0007]

[MEANS OF SOLUTION OF THE PROBLEM] FIG.1 shows the principle of the present invention. In the drawing, 1 represents a semiconductor chip, 2 represents a wiring pad, 3 represents a conductor film, 4 represents a guard ring, 5 represents a linear pattern, and 6 represents a bending point.

[0008] In order to solve the foregoing problem, the present invention reduces the straight part 5 of the guard ring 4 provided along the rim of the semiconductor chip by providing a plurality of bending points 6.

[0009] Thus, the object of the present invention is to provide the guard ring 4 of the conductor film 3 between the rim of the semiconductor chip 1 and the wiring pad 2 in a zigzag pattern or curved pattern as represented in FIG.1. Alternatively, the present invention achieves the object thereof by forming the guard ring 4 by a plural layers of the conductor film 3, the upper conductor film 3 and the lower conductor film 3 being connected via a through-hole 8

formed in an interlayer insulation film 7. Alternatively, the present invention achieves the object by forming the conductor film 3 such that an upper conductor film 3a covers entirely a lower conductor film 3b.

[0010]

[FUNCTION] According to the means of the present invention, the straight pattern of the conductor film constituting the guard ring is reduced by way of providing a number of bending points. Thus, the short straight pattern portions bear the stress, and thus, the large stress is effectively distributed. Further, the plurality of the bending point absorbs the stress due to the resilient nature thereof and the crack formation is reduced.

[0011]

[EMBODIMENT] FIG.2 shows an embodiment of the present invention in a schematic view. In the drawing, 1 represents a semiconductor chip, 2 represents a wiring pad, 3 represents a conductor film, 3a represents an upper conductor film, 3b represents a lower conductor film, 7 represents an interlayer insulation film, 8 represents a through-hole, 9 represents four corners and 11 represents a Si substratye.

[0012] Hereinafter, an embodiment of the present invention will be explained with reference to FIG.2. As

indicated in FIG.2(a), the guard ring 4 includes an upper conductor film 3a of a polysilicon film and a lower conductor film 3b of an Al film separated from each other by the interlayer insulation film 7 of SiO_2 with a distance of about 50 μm. The interlayer insulation film 7 is formed with a through-hole (contact window) 8 so as to connect the upper conductor film 3a and the lower conductor film 3b.

[0013] The straight pattern portion 5 of the guard ring 4 is reduced as much as possible, by providing a large number of bending points 6. In the illustrated example, the interior angle of the bending point 6 is set to 135° . It is preferable to form the bending points 6 in the form of a polygon, which is close to a circle.

[0014] FIG.2(b) shows a cross-sectional view taken along a line A-A' of FIG.2(a). It can be seen that the upper conductor film 3a covering the lower conductor film 3b extends outside the lower conductor film 3b. In such a structure, a large stress applied fro the four corners 9 of the chip is distributed into short straight pattern portions 5 of the guard ring 4. Further, the series a - a" and the series c - c" perform a resilient action and the cracking of the passivation film covering the lower conductor film 3b not illustrated or the disconnection of the guard ring 4 is prevented.

[0015]

[EFFECT OF THE INVENTION] According to the present invention, the stress applied to the passivation film is reduced by reducing the length of the straight portion of a thin guard ring, in which formation of a slit is difficult and by forming a plurality of bending points. Thus, the probability of guard ring disconnection is reduced and the performance degradation of a semiconductor device caused by an external stress is improved together with the moisture resistance. Thus, the present invention contributes to the improvement of reliability of a semiconductor device.

[BRIEF EXPLANATION OF THE DRAWINGS]

[FIG.1] The drawing shows the principle of the present invention.

[FIG.2] The drawing shows an embodiment of the present invention.

[FIG.3] The drawing shows a prior art.

[EXPLANATION OF REFERENCE NUMERALS]

1 semiconductor chip

2 wiring pad

3 conductor film

3a upper conductor film

3b lower conductor film

4 guard ring

5	straight pattern
6	bending point
7	interlayer insulation film
10,8	through-hole
11	Si substrate